



## REMARKS

Claims 1-11 are pending. The indication of allowable subject matter with respect to claims 5-11 is appreciated.

Claims 1 -4 were rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Applicant’s admitted prior art in view of Hamaguchi et al. (*hereafter*: Hamaguchi). The Applicant respectfully traverses this rejection for the following reason(s).

Applicant's admitted prior art comprises all that is claimed in claim 1 except the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*, which is deemed to be non-obvious in view of the proposed combination of art.

It noted here that the Examiner has not identified where the foregoing feature of claim 1 is found in the applied art. Note, *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990) states:

"it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

The Examiner relies on other case law, see paragraph 7 on pages 6-7 of Paper No. 8, to suggest that the references need not explicitly **provide motivation** for combining the teachings

thereof, and to further suggest that the "examiner may provide an explanation based on logic and sound scientific reasoning that will support a holding of obviousness." The Examiner has **not** provided any sound scientific reasoning nor logical explanation of how the combination of references teach the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*. The Applicant has not argued the issue of motivation to combine Applicant's admitted prior art and Hamaguchi. The Applicant readily admitted:

"There is no doubt that Hamaguchi's power regulatory circuitry would protect the CRT display of the Applicant's admitted prior art" (page 3, lines 8-9 of the response filed 1/7/00)

The Applicant, however, argues that the combination would not protect the CRT display by *gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*, and the Examiner has not identified where this aspect of the claimed invention is taught by the combined art. The Examiner appears to be confusing **motivation and limitations**. The Examiner fails to identify any case law which permits the Office to ignore limitations of the claims, because there is no such case law.

*In re Ochiai*, 71 F.3d 1565, 37 USPQ2d 1127 (Fed. Cir. 1995):

"The test for obviousness vel non is statutory. It requires that one compare the claim's 'subject matter as a whole' with the prior art 'to which said subject matter pertains.' 35 U.S.C. §103. The inquiry is

thus highly fact-specific by design."

On page 6 of Paper No. 8 the Examiner states, "Hamaguchi et al. does not have to explicitly said that "gradually lowering said input voltage". Since circuit 16 of Hamaguchi et al. is equivalent to the power interruption circuitry claimed by the applicant." The Examiner is correct that Hamaguchi does not have to explicitly state "gradually lowering said input voltage," however the art **must** provide some teaching to suggest to one of ordinary skill in the art the feature of *gradually lowering said input voltage*. . . The Examiner errs in stating that " circuit 16 of Hamaguchi et al. is equivalent to the power interruption circuitry claimed by the applicant." Hamaguchi's CRT protection circuit utilizes an overvoltage/overcurrent detector 30 and control circuit 40 to control the turning off a horizontal output transformer Qa "instantaneously" upon detection of an abnormal state. See col. 2, lines 40-47. Circuit 16 of Hamaguchi is merely a rectifier that rectifies the high voltage output from transformer 15 before passing the high voltage on to the anode of the CRT, and has no other function. Circuit (rectifier) 16 is, therefore, **not** equivalent to the *power interruption delay charging means* claimed by the applicant. Accordingly, neither the Applicant's admitted prior art nor Hamaguchi teach or suggest *gradually lowering an input voltage*, and the Examiner has not provided a *prima facie* showing that one of ordinary skill in the art would have been motivated to provide *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*.

As noted above, the Examiner has **not** provided any sound scientific reasoning nor logical

explanation of how the combination of references teach the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*. Instead, the Examiner erroneously suggests equivalency with respect to the Applicant's claimed *power interruption delay charging means* and circuit 16 of Hamaguchi, which is a rectifier, not a CRT protection circuit, that rectifies the current output from a flyback transformer to obtain a high voltage (HV). Rectifier 16 of Hamaguchi does not have the function nor the capability to perform the function of *gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*. At no point does the Examiner provide any logical explanation nor scientific reasoning to support the rejection. Instead, the Examiner has merely suggested using Hamaguchi's power regulatory circuitry with Applicant's admitted prior art "because it would protect the CRT display" without any explanation of how Hamaguchi's power regulatory circuitry would be made to perform the function of *gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*. Accordingly, circuit 16 of Hamaguchi is not equivalent to the claimed *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*.

As noted above, the issue is not one of "motivation to combine," but is instead one of whether the claim, as a whole, is taught by the combined prior art. Since the art fails to teach the **whole** feature of *power interruption delay charging means for gradually lowering said input*

*voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*, then the rejection is in error.

Accordingly, the rejection of claims 1-4 is deemed to be in error and should be withdrawn.

The examiner is respectfully requested to reconsider the application, withdraw the objections and/or rejections and pass the application to issue in view of the above amendments and/or remarks.

No fee is incurred by this Response.

Respectfully submitted,

  
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